REMARKS

Claims 1-8, 10 and 12 are pending in this application. By this amendment, Applicants amend claims 1 and 10 and cancel claims 9, 11 and 13-17.

Claims 1-8, 10 and 12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kuriyama et al. (U.S. 6,068,499) in view of Applicants' Admitted Prior Art Figure 8 (AAPA). This rejection is respectfully traversed.

Claim 1 recites:

> "A method of producing a high frequency circuit chip having a substrate made of a ceramic with a high dielectric constant, a wiring pattern provided on one main surface of the substrate, an electric conductor layer provided on substantially all of another main surface of the substrate, and a through-hole including a connecting electrode for connecting the wiring pattern and the conductor layer to each other, the method comprising the steps of:
>
> **filling electrically conductive paste into a perforation in the substrate, and firing the paste to form the connecting electrode of the through-hole;**
>
> **forming a resist pattern with an opening having a desired shape and size directly on the substrate;**
>
> **forming a thin film with a wiring material directly on the substrate through the opening over the resist pattern after forming the resist pattern; and**
>
> **removing the unnecessary wiring material thin film deposited on the resist pattern together with the resist pattern to form the wiring pattern directly on the substrate by a lift-off method."** (Emphasis added)

Claim 10 recites method steps that are similar to claim 1, including the emphasized method steps.

The Examiner alleged that Kitamura et al. teaches all of the method steps recited in claims 1 and 10, except for using a conductive paste. However, the Examiner further alleged that AAPA teaches in Fig. 8 a conductive paste 60. Thus, the Examiner concluded that it would have been obvious to use conductive paste as taught by AAPA in Kitamura et al.'s device "in order to pattern and manipulate the conductive material with more ease." Applicants respectfully disagree.

In contrast to the present claimed invention and the Examiner's allegations,

Kitamura et al. teaches a method including the steps of forming a surface layer conductor 901 "having no patterning" on the **entire** upper surface of the substrate 900, forming a resist pattern 903 **only** on the upper surface of the surface layer conductor 901 (and clearly **not** on any portion of the substrate 900), forming via conductors 904 on the surface layer conductor 901, forming another resist pattern 905 on portions of the surface layer conductor 901 and the via conductors 904 (but clearly **not** on any portion of the substrate 900), and **then** removing portions of the surface layer conductor 901. Thus, Kitamura et al. clearly fails to teach or suggest the steps of "forming a resist pattern with an opening having a desired shape and size **directly on the substrate,**" "forming a thin film with a wiring material **directly on the substrate through the opening over the resist pattern** after forming the resist pattern," and "removing the unnecessary wiring material thin film deposited on the resist pattern together with the resist pattern to form the wiring pattern directly on the substrate by a lift-off method" (emphasis added) as recited in the present claimed invention.

Therefore, the method of Kitamura et al. teaches the steps of forming **a resist pattern after** forming the surface layer conductor, which is the exact opposite of the present claimed method including the step of "**forming a thin film with a wiring material after** forming the resist pattern."

The Examiner alleged that Kitamura et al. teaches the steps of filling electrically conductive material into a perforation in the substrate, and firing the conductor to form the connecting electrode in the through hole. However, contrary to the Examiner's allegations, Kitamura et al. clearly and specifically teaches that the through hole shown in Figs. 9a-9g is filled with an **insulating** film 902, **NOT** with a **conductive** material (see the paragraph bridging cols. 11 and 12 of Kitamura et al.). Thus, Kitamura et al. clearly fails to teach or suggest "filling electrically conductive paste into a perforation in the substrate" as recited in the present claimed invention.

In addition, Kitamura et al. fails to teach or suggest **any** step of firing the material filled into the perforation in the substrate, and certainly fails to teach or suggest the step of "firing th paste to form the connecting electrode of the through-hole" as recited in the present claimed invention.

The Examiner further alleged that "although figures 9a-9g [of Kitamura et al.] do not depict a wiring material over the resist pattern, it is well known in the art that a wiring material is deposited on the entire surface of the substrate, including the resist pattern. Therefore, Kitamura et al. teach a wiring material being deposited on the entire surface of the substrate, including the resist pattern, as claimed." Applicants are bewildered by the Examiner's allegation. Figs. 9a-9g of Kitamura et al. illustrate the complete method of forming a wiring pattern on a substrate, and, as acknowledged by the Examiner, none of these figures teaches or suggests a step of depositing a wiring material on the entire surface of the substrate, including the resist pattern. Yet, the Examiner has somehow concluded Kitamura et al. teaches this undisclosed step. This is clearly incorrect. Prior art rejections must be based on evidence. Graham v. John Deere Co., 383 U.S. 117 (1966). Here, the Examiner has clearly failed to provide any reference which teaches or suggests the method step identified above. Accordingly, Applicants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness.

Alternatively, the Examiner alleged that it would have been obvious to deposit the wiring material on the entire surface of the substrate, including the resist pattern in Kitamura et al.'s device in order to simplify the processing steps of making the device. However, neither Kitamura et al. nor AAPA teaches or suggest that such a depositing step would simplify the processing steps, and the Examiner has completely failed to explain how or in what manner such a depositing step would simplify the processing steps or why such step is even necessary in the complete method taught by Kitamura et al. Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination. In re Geiger, 815 F.2d 686, 2 USPQ 1276, 1278 (Fed. Cir. 1987).

The Examiner further alleged that it would have been obvious to use the conductive paste of AAPA in Kitamura et al.'s device "in order to pattern and manipulate the conductive material with more ease." However, neither Kitamura et al. nor AAPA teaches or suggest that the use of conductive paste would facilitate the patterning and manipulation of the conductive material, and the Examiner has completely failed to

explain how or in what manner the use of conductive paste would facilitate the patterning and manipulation of the conductive material. Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination. In re Geiger, 815 F.2d 686, 2 USPQ 1276, 1278 (Fed. Cir. 1987).

In addition, Kitamura et al. clearly teaches away from filling a perforation with conductive paste, as opposed to an insulating film 902, because to substitute the conductive paste of AAPA for the insulating film 902 of Kitamura et al. would render the device of Kitamura et al. inoperative since the neighboring conductive patterns as seen in Figs. 9a-9g of Kitamura et al. would be short-circuited. It is error to find obviousness where references diverge and teach away from the invention at hand. W.L. Gore & Assoc. v. Garlock Inc., 721 F .2d 1540, 1550, 220 USPQ 303, 311 (Fed. Cir. 1983).

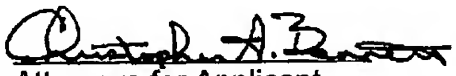
Accordingly, Applicants respectfully submit that Kitamura et al. and AAPA, applied alone or in combination, fail to teach or suggest the unique combination of method steps recited in claims 1 and 10 of the present invention.

In view of the foregoing amendments and remarks, Applicants respectfully submit that claims 1 and 10 are allowable. Claims 2-8 and 12 depend upon claims 1 and 10, and are therefore allowable for at least the reasons that claims 1 and 10 are allowable.

In view of the foregoing Remarks, Applicants respectfully submit that this application is in condition for allowance. Favorable consideration and prompt allowance are respectfully solicited.

The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,



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